

# AS5115

## Programmable 360° Magnetic Angle Encoder with Buffered Sine and Cosine Output Signals

### General Description

The AS5115 is a contactless rotary encoder sensor for accurate angular measurement over a full turn of 360° and over an extended ambient temperature range of -40°C to 150°C.

Based on an integrated Hall element array, the angular position of a simple two-pole magnet is translated into analog output voltages. The angle information is provided by means of buffered sine and cosine voltages. This approach gives maximum flexibility in system design, as it can be directly integrated into existing architectures and optimized for various applications in terms of speed and accuracy.

An SSI Interface is implemented for signal path configuration as well as a one time programmable register block (OTP), which allows the customer to adjust the signal path gain to adjust for different mechanical constraints and magnetic field.

*Ordering Information and Content Guide appear at end of datasheet.*

### Key Benefits & Features

The benefits and features of AS5115, Programmable 360° Magnetic Angle Encoder with Buffered Sine and Cosine Output Signals are listed below:

**Figure 1:**  
**Added Value of Using AS5115**

| Benefits                             | Features                                                                                   |
|--------------------------------------|--------------------------------------------------------------------------------------------|
| • Highest reliability and durability | • Contactless high resolution rotational position encoding over a full turn of 360 degrees |
| • Simple programming                 | • Simple user-programmable over serial interface (SSI)                                     |
| • High precision analog output       | • Buffered sine and cosine output signals                                                  |
| • Very low average power consumption | • Low Power mode                                                                           |
| • Easy setup                         | • Serial read-out of multiple interconnected devices using daisy chain mode                |
| • Fully automotive qualified         | • AEC-Q100, grade 0                                                                        |
| • Small form factor                  | • SSOP 16                                                                                  |
| • Robust environmental tolerance     | • Wide temperature range: -40°C to 150°C                                                   |

## Applications

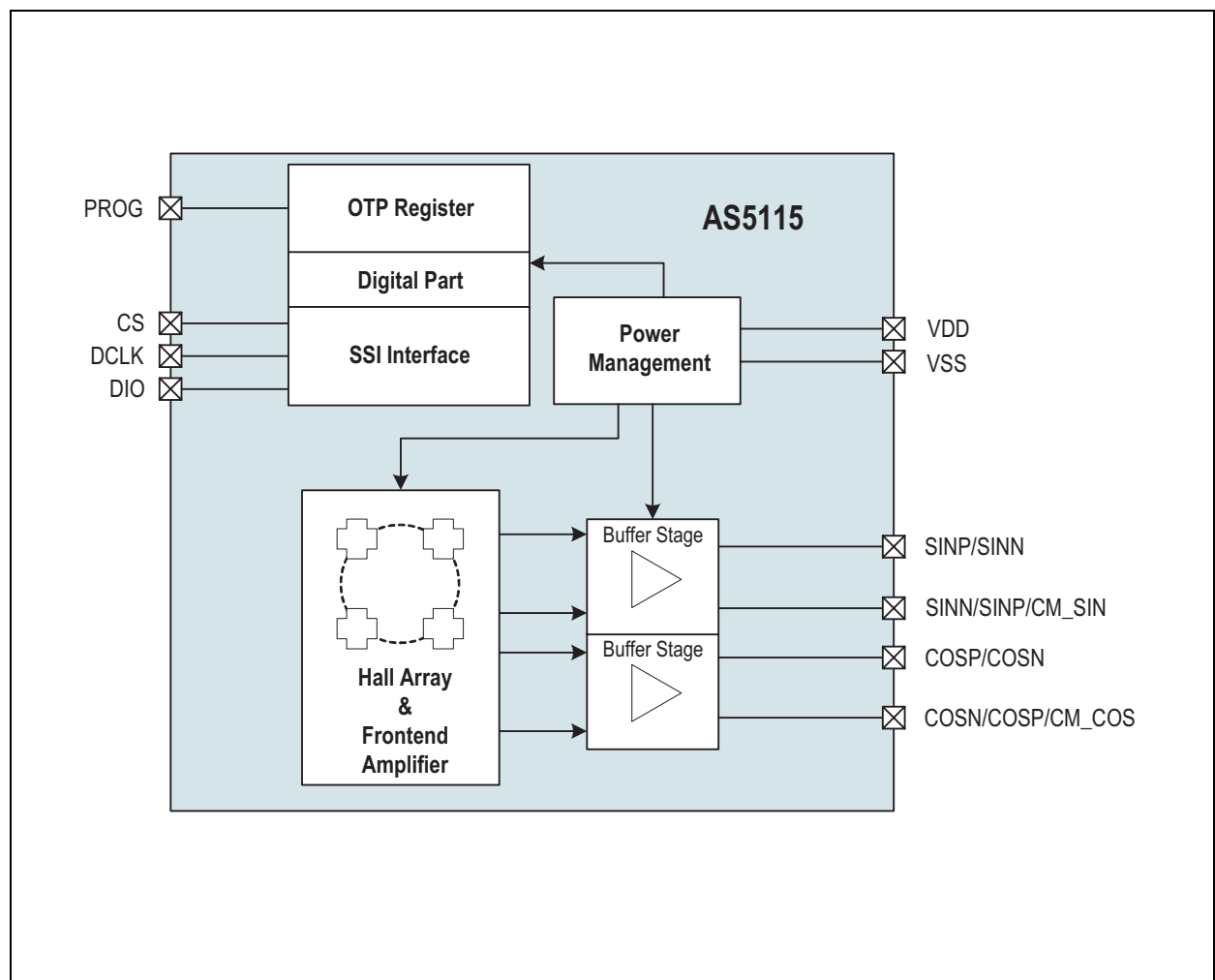
The AS5115 is ideal for several automotive and industrial applications such as

- Microcontroller-based systems
- Contactless rotary position sensing
- General purpose for automotive and industrial applications

## Block Diagram

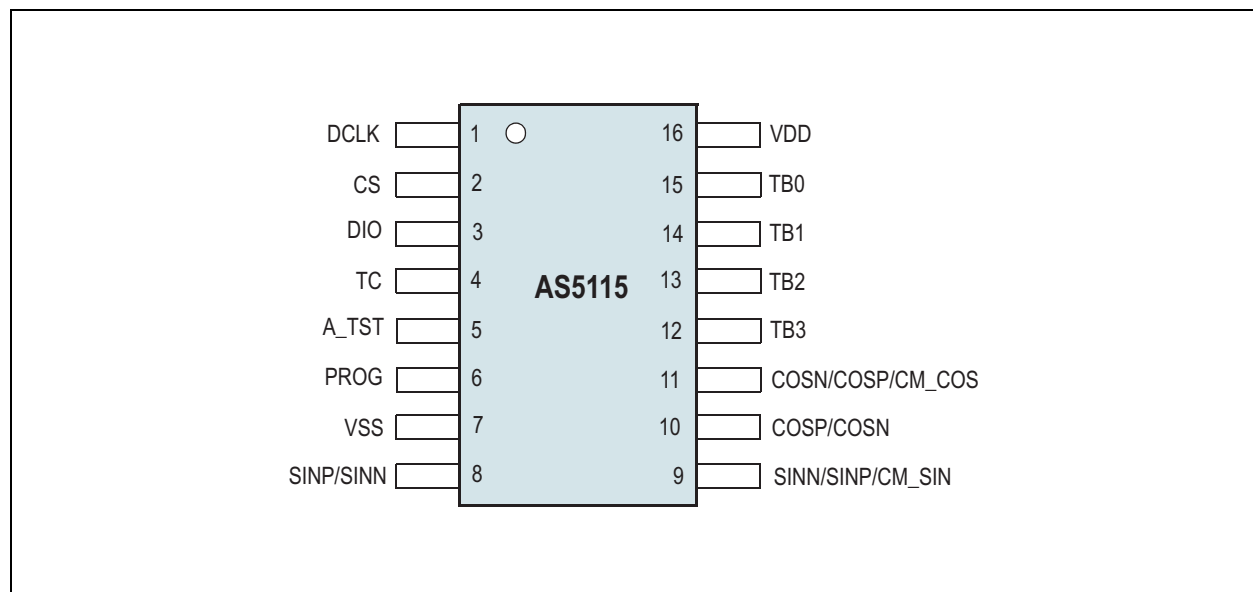
The functional blocks of this device are shown below:

**Figure 2:**  
**AS5115 Block Diagram**



## Pin Assignments

**Figure 3:**  
**Pin Diagram (Top View)**



## Pin Description

**Figure 4:**  
**Pin Description**

| Pin Name         | Pin Number | Pin Type                           | Description                                            |
|------------------|------------|------------------------------------|--------------------------------------------------------|
| DCLK             | 1          | Digital input with Schmitt trigger | Clock input for digital interface                      |
| CS               | 2          |                                    | Clock input for digital interface, Scan enable         |
| DIO              | 3          | Digital input/output               | Data I/O for digital interface, Scan input             |
| TC               | 4          | Analog input/output                | Test coil                                              |
| A_TST            | 5          | Analog output/Digital output       | Analog test pin, Scan output                           |
| PROG             | 6          | Supply pad                         | OTP programming pad                                    |
| VSS              | 7          |                                    | Also used as VSS of test coil + EasyZapp (double bond) |
| SINP/SINN        | 8          | Analog output                      | Buffered analog output                                 |
| SINN/SINP/CM_SIN | 9          |                                    |                                                        |
| COSP/COSN        | 10         |                                    |                                                        |
| COSN/COSP/CM_COS | 11         |                                    |                                                        |

| Pin Name | Pin Number | Pin Type                    | Description                                                |
|----------|------------|-----------------------------|------------------------------------------------------------|
| TB3      | 12         | Analog output/Digital input | Test bus, analog output                                    |
| TB2      | 13         |                             |                                                            |
| TB1      | 14         |                             | Test bus, analog output; external clock → sync. prod. test |
| TB0      | 15         | Analog output               | Test bus, analog output                                    |
| VDD      | 16         | Supply pad                  | Digital + analog supply                                    |

## Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Operating Conditions](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 5:**  
**Absolute Maximum Ratings**

| Symbol                                    | Parameter                        | Min  | Max                   | Units | Comments                                                                                                                                                                                                                                                                                              |
|-------------------------------------------|----------------------------------|------|-----------------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Electrical Parameters                     |                                  |      |                       |       |                                                                                                                                                                                                                                                                                                       |
| V <sub>DD</sub>                           | Supply voltage                   | -0.3 | 7                     | V     |                                                                                                                                                                                                                                                                                                       |
| V <sub>in</sub>                           | Input pin voltage                | -0.3 | V <sub>DD</sub> + 0.3 | V     |                                                                                                                                                                                                                                                                                                       |
| I <sub>scr</sub>                          | Input current (latchup immunity) | -100 | 100                   | mA    | EIA/JESD78 Class II Level A                                                                                                                                                                                                                                                                           |
| Electrostatic Discharge                   |                                  |      |                       |       |                                                                                                                                                                                                                                                                                                       |
| ESD <sub>HBM</sub>                        | Electrostatic discharge          | ±2   |                       | kV    | JESD22-A114E                                                                                                                                                                                                                                                                                          |
| Continuous Power Dissipation              |                                  |      |                       |       |                                                                                                                                                                                                                                                                                                       |
| P <sub>tot</sub>                          | Total power dissipation          |      | 275                   | mW    |                                                                                                                                                                                                                                                                                                       |
| Q <sub>JA</sub>                           | Package thermal resistance       |      | 110                   | °C/W  | Velocity =0; Multi Layer PCB; Jedec Standard Testboard                                                                                                                                                                                                                                                |
| Temperature Ranges and Storage Conditions |                                  |      |                       |       |                                                                                                                                                                                                                                                                                                       |
| T <sub>strg</sub>                         | Storage temperature              | -65  | 150                   | °C    |                                                                                                                                                                                                                                                                                                       |
| T <sub>body</sub>                         | Package body temperature         |      | 260                   | °C    | IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices”. The lead finish for Pb-free leaded packages is matte tin(100% Sn). |
| RH <sub>NC</sub>                          | Relative humidity non-condensing | 5    | 85                    | %     |                                                                                                                                                                                                                                                                                                       |
| MSL                                       | Moisture sensitivity level       | 3    |                       |       | Represents a maximum floor time of 168h                                                                                                                                                                                                                                                               |

## Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

**Figure 6:**  
Operating Conditions

| Symbol    | Parameter               | Conditions | Min | Typ | Max | Unit |
|-----------|-------------------------|------------|-----|-----|-----|------|
| $V_{DD}$  | Positive supply voltage |            | 4.5 |     | 5.5 | V    |
| $V_{SS}$  | Negative supply voltage |            | 0.0 |     | 0.0 | V    |
| $T_{amb}$ | Ambient temperature     |            | -40 |     | 150 | °C   |

**Figure 7:**  
DC/AC Characteristics for Digital Inputs and Outputs

| Symbol                      | Parameter                 | Conditions | Min                | Typ | Max                | Unit    |
|-----------------------------|---------------------------|------------|--------------------|-----|--------------------|---------|
| <b>CMOS Input</b>           |                           |            |                    |     |                    |         |
| $V_{IH}$                    | High level input voltage  |            | $0.7 \cdot V_{DD}$ |     | $V_{DD}$           | V       |
| $V_{IL}$                    | Low level input voltage   |            | 0                  |     | $0.3 \cdot V_{DD}$ | V       |
| $I_{LEAK}$                  | Input leakage current     |            |                    |     | 1                  | $\mu A$ |
| <b>CMOS Output</b>          |                           |            |                    |     |                    |         |
| $V_{OH}$                    | High level output voltage | 4mA        | $V_{DD} - 0.5$     |     | $V_{DD}$           | V       |
| $V_{OL}$                    | Low level output voltage  | 4mA        | 0                  |     | $V_{SS} + 0.4$     | V       |
| $C_L$                       | Capacitive load           |            |                    |     | 35                 | pF      |
| <b>CMOS Output Tristate</b> |                           |            |                    |     |                    |         |
| $I_{OZ}$                    | Tristate leakage current  |            |                    |     | 1                  | $\mu A$ |

**Figure 8:**  
Magnetic Input Specification

| Symbol       | Parameter                      | Conditions                                          | Min | Typ | Max | Unit |
|--------------|--------------------------------|-----------------------------------------------------|-----|-----|-----|------|
| $B_{Zpp}$    | Magnetic input field amplitude | Peak to peak at the radius (=1mm) of the hall array | 32  |     | 160 | mT   |
| $B_{offset}$ | Magnetic field offset          | Within the linear range of the magnet               | -10 |     | 10  | mT   |
| $f_{rot}$    | Rotational speed               | Maximum 30,000 RPM                                  | 0   |     | 500 | Hz   |

**Figure 9:**  
**Electrical System Specifications**

| Symbol                    | Parameter                                      | Conditions                                                                                             | Min                    | Typ  | Max                   | Unit    |
|---------------------------|------------------------------------------------|--------------------------------------------------------------------------------------------------------|------------------------|------|-----------------------|---------|
| IDD                       | Current consumption                            | Maximum value derived at maximum I <sub>H</sub> (Hall Bias Current)                                    |                        |      | 28                    | mA      |
| t <sub>power_on</sub>     | Power up time                                  |                                                                                                        |                        |      | 1.275                 | ms      |
| t <sub>prop</sub>         | Propagation delay                              | -40°C to 150°C                                                                                         | 18                     | 22   | 30                    | μs      |
| M                         | Magnetic sensitivity                           | Version: AS5115                                                                                        | 10                     |      | 60                    | mV / mT |
|                           |                                                | Version: AS5115A                                                                                       | 20.72                  | 28   | 35.28                 |         |
|                           |                                                | Version: AS5115F                                                                                       | 13.5                   | 24   | 34.5                  |         |
| V <sub>PP</sub>           | Analog output voltage amplitude (peak to peak) |                                                                                                        | 1.38                   | 1.94 | 2.5                   | V       |
| AM <sub>Temp</sub>        | AM tracking accuracy over temperature          | -40°C to 150°C                                                                                         | -1                     |      | 1                     | %       |
| AM                        | Sin / Cos amplitude mismatch                   | 25°C                                                                                                   | -2                     |      | 2                     | %       |
| V <sub>offset1</sub>      | Output DC offset voltage                       | At no input signal; programmable OTP setting (see <a href="#">Device Communication / Programming</a> ) | 1.47                   | 1.5  | 1.53                  | V       |
| V <sub>offset2</sub>      |                                                |                                                                                                        | 2.45                   | 2.5  | 2.55                  |         |
| DC <sub>offsetdrift</sub> | DC offset drift                                | -40°C to 150°C                                                                                         | -50                    |      | 50                    | μV/°C   |
| V <sub>OUT</sub>          | Analog output range                            |                                                                                                        | V <sub>SS</sub> + 0.25 |      | V <sub>DD</sub> - 0.5 | V       |
| I <sub>OUT</sub>          | Output current                                 |                                                                                                        | -1                     |      | 1                     | mA      |
| C <sub>LOAD</sub>         | Capacitive load                                |                                                                                                        |                        |      | 1000                  | pF      |

## Timing Characteristics

**Figure 10:**  
Timing Characteristics

| Symbol | Parameter                                                                | Condition                            | Min                               | Typ | Max                                | Unit |
|--------|--------------------------------------------------------------------------|--------------------------------------|-----------------------------------|-----|------------------------------------|------|
| t1_3   | Chip select to positive edge of DCLK                                     | see<br>Figure 18<br>and<br>Figure 19 | 30                                |     |                                    | ns   |
| t2_3   | Chip select to drive bus externally                                      |                                      | 0                                 |     |                                    | ns   |
| t3     | Setup time command bit Data valid to positive edge of DCLK               |                                      | 30                                |     |                                    | ns   |
| t4     | Hold time command bit Data valid after positive edge of DCLK             |                                      | 15                                |     |                                    | ns   |
| t5     | Float time positive edge of DCLK for last command bit to bus float       |                                      |                                   |     | $\frac{1}{(2 + 0) \cdot f\_DCLK}$  | ns   |
| t6     | Bus driving time Positive edge of DCLK for last command bit to bus drive |                                      | $\frac{1}{(2 + 0) \cdot f\_DCLK}$ |     |                                    | ns   |
| t7     | Data valid time positive edge of DCLK to bus valid                       |                                      | $\frac{1}{(2 + 0) \cdot f\_DCLK}$ |     | $\frac{1}{(2 + 30) \cdot f\_DCLK}$ | ns   |
| t8     | Hold time data bit Data valid after positive edge of DCLK                |                                      | $\frac{1}{(2 + 0) \cdot f\_DCLK}$ |     |                                    | ns   |
| t9_3   | Hold time chip select positive edge DCLK to negative edge of chip select |                                      | $\frac{1}{(2 + 0) \cdot f\_DCLK}$ |     |                                    | ns   |

| Symbol | Parameter                                                                          | Condition | Min | Typ | Max | Unit |
|--------|------------------------------------------------------------------------------------|-----------|-----|-----|-----|------|
| t10_3  | Bus floating time<br>negative edge of chip<br>select to float bus                  |           |     |     | 30  | ns   |
| t11    | Setup time data bit at<br>write access<br>Data valid to positive<br>edge of DCLK   |           | 30  |     |     | ns   |
| t12    | Hold time data bit at<br>write access<br>Data valid after positive<br>edge of DCLK |           | 15  |     |     | ns   |
| t13_3  | Bus floating time<br>negative edge of chip<br>select to float bus                  |           | -   |     | 30  | ns   |

**Note(s):**

1. The digital interface will be reset during the low phase of the CS signal.

## Detailed Description

### Sleep Mode

The target is to provide the possibility to reduce the total current consumption. No output signal will be provided when the IC is in sleep mode. Enabling or disabling sleep mode is done by sending the SLEEP or WAKEUP commands via the SSI interface. Analog blocks are powered down with respect to fast wake up time.

### SSI Interface

The setup for the device is handled by the digital interface. Each communication starts with the rising edge of the chip select signal. The synchronization between the internal free running analog clock oscillator and the external used digital clock source for the digital interface is done in a way that the digital clock frequency can vary in a wide range.

**Figure 11:**  
SSI Interface Pin Description

| Port                            | Symbol | Function                                                                                                           |
|---------------------------------|--------|--------------------------------------------------------------------------------------------------------------------|
| Chip select                     | CS     | Indicates the start of a new access cycle to the device.<br>CS = LO → reset of the digital interface               |
| DCLK                            | DCLK   | Clock source for the communication over the digital interface.                                                     |
| Bidirectional data input output | DIO    | Command and data information over one single line.<br>The first bit of the command defines a read or write access. |

**Figure 12:**  
**SSI Interface Parameter Description**

| Symbol    | Parameter                                     | Notes                                                                                                                                                                                                      | Min      | Typ   | Max   | Unit |
|-----------|-----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-------|-------|------|
| f_DCLK    | Clock frequency at normal operation           | The nominal value for the clock frequency can be derived from a 10MHz oscillator source.                                                                                                                   | No limit | 5     | 6     | MHz  |
| f_EZ_RW   | Clock frequency at easy zap read write access |                                                                                                                                                                                                            | No limit | 5     | 6     | kHz  |
| f_EZ_PROG | Clock frequency at easy zap accessprogram OTP | Correct access to the programmable zener diode block needs a strict timing – the zappulse is exact one period.<br>The nominal value for the clock frequency can be derived from a 10MHz oscillator source. | 200      |       | 650   | kHz  |
| f_EZ_ARB  | Clock frequency at easy zap analog readback   | 20pF external load allowed.<br>The nominal value for the clock frequency can be derived from a 10MHz oscillator source.                                                                                    | No limit | 156.3 | 162.5 | kHz  |

| Parameter                                      | Notes                                    |
|------------------------------------------------|------------------------------------------|
| <b>Interface General at Normal Mode</b>        |                                          |
| Protocol: 5 command bit + 16 data input output |                                          |
| Command                                        | 5-bit command: cmd<4:0> ← bit<21:16>     |
| Data                                           | 16-bit data: data<15:0> ← bit<15:0>      |
| <b>Interface General at Extended Mode</b>      |                                          |
| Protocol: 5 command bit + 46 data input output |                                          |
| Command                                        | 5-bit command: cmd<4:0> ← bit<50:46>     |
| Data                                           | 34-bit data: data<45:0> ← bit<45:0>      |
| <b>Interface Modes</b>                         |                                          |
| Normal read operation mode                     | cmd<4:0> = <00xxx> → 1 DCLK per data bit |
| Extended read operation mode                   | cmd<4:0> = <01xxx> → 4 DCLK per data bit |
| Normal write operation mode                    | cmd<4:0> = <10xxx> → 1 DCLK per data bit |
| Extended write operation mode                  | cmd<4:0> = <11xxx> → 4 DCLK per data bit |

## Device Communication / Programming

**Figure 13:**  
Digital Interface at Normal Mode

| #  | Command      | Bin   | Mode  | 15       | 14      | 13 | 12 | 11 | 10 | 9          | 8           | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|--------------|-------|-------|----------|---------|----|----|----|----|------------|-------------|---|---|---|---|---|---|---|---|
| 23 | WRITE_CONFIG | 10111 | write | go2sleep | gen_rst |    |    |    |    | analog_sig | OB_bypassed |   |   |   |   |   |   |   |   |
| 16 | EN_PROG      | 10000 | write | 1        | 0       | 0  | 0  | 1  | 1  | 0          | 0           | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |

| Name        | Functionality                                        |
|-------------|------------------------------------------------------|
| go2sleep    | Enter/leave low power mode (no output signals)       |
| gen_rst     | Generates global reset                               |
| analog_sig  | Switches the channels to the test bus after the PGA  |
| OB_bypassed | Disable and bypass output buffer for testing purpose |

**Figure 14:**  
**Digital Interface at Extended Mode**

| #  | Command    | Bin   | Mode     | Factory Settings |             |             |             |             |             |      |      | User Settings      |            |            |           |               |               |
|----|------------|-------|----------|------------------|-------------|-------------|-------------|-------------|-------------|------|------|--------------------|------------|------------|-----------|---------------|---------------|
|    |            |       |          | <45:<br>44>      | <43:<br>26> | <25:<br>23> | <22:<br>20> | <19:<br>18> | <17:<br>14> | <13> | <12> | <11>               | <10>       | <9>        | <8:<br>7> | <6>           | <5:<br>0>     |
| 31 | WRITE_OTP  | 11111 | xt write | r                | r           | r           | r           | r           | r           | r    | r    | invert_<br>channel | cm_<br>sin | cm_<br>cos | gain      | dc_<br>offset | hall_<br>bias |
| 25 | PROG_OTP   | 11001 | xt write | r                | r           | r           | r           | r           | r           | r    | r    | invert_<br>channel | cm_<br>sin | cm_<br>cos | gain      | dc_<br>offset | hall_<br>bias |
| 15 | RD_OTP     | 01111 | xt read  | r                | r           | r           | r           | r           | r           | r    | r    | invert_<br>channel | cm_<br>sin | cm_<br>cos | gain      | dc_<br>offset | hall_<br>bias |
| 9  | RD_OTP_ANA | 01001 | xt read  |                  |             |             |             |             |             |      |      |                    |            |            |           |               |               |

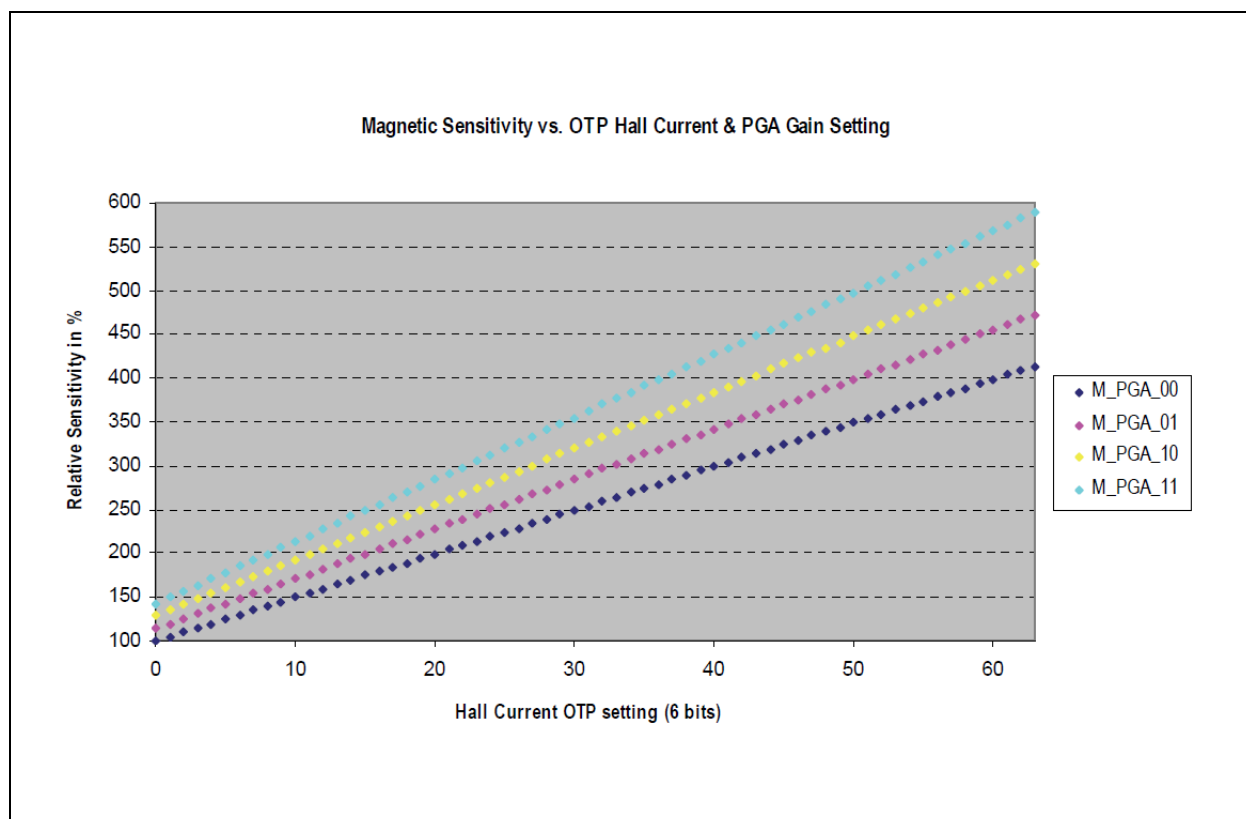
**Note(s):**

1. "r" stands for reserved bits. They must not be modified, unless otherwise noted.
2. Send EN PROG (command 16) in normal mode before accessing the OTP in extended mode.
3. OTP assignment will be defined/updated.

**Figure 15:**  
User Settings Description

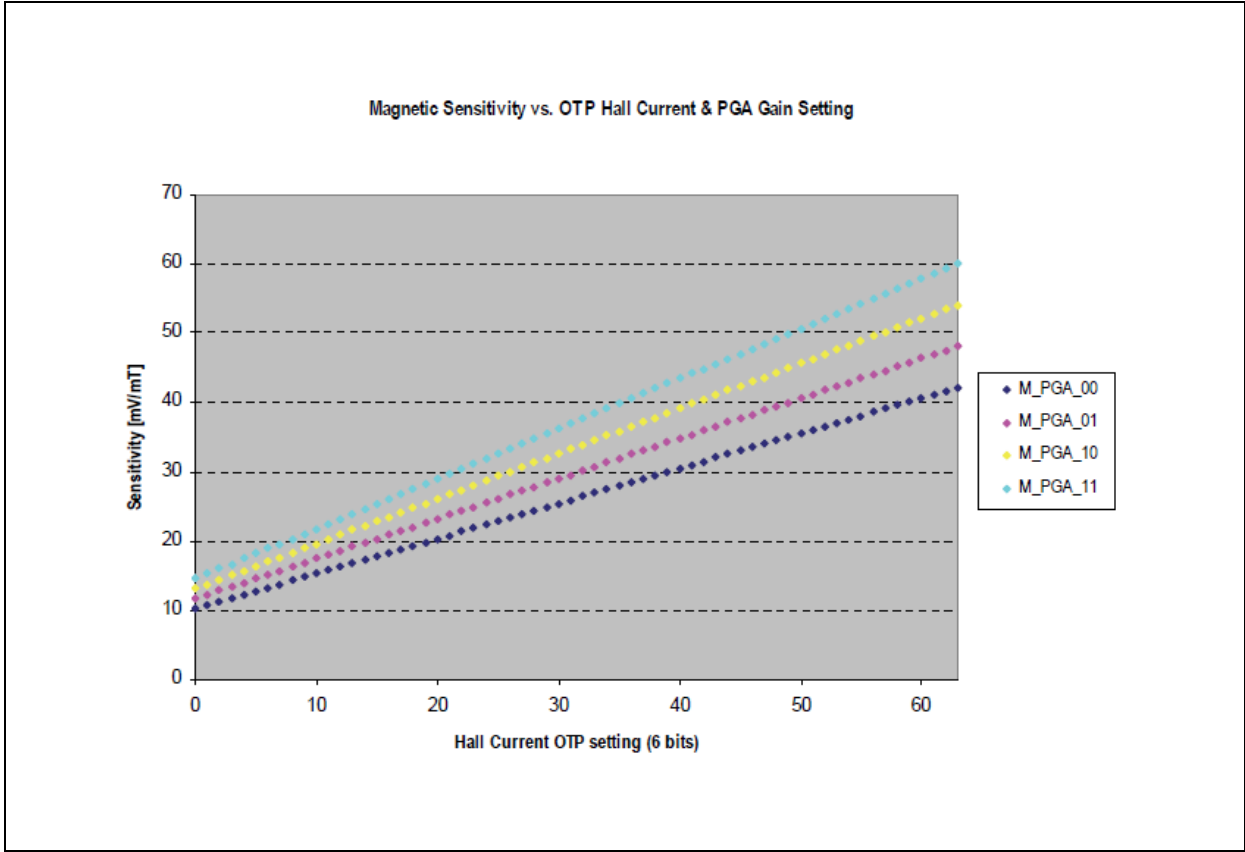
| Name                   | Functionality                                                                                |
|------------------------|----------------------------------------------------------------------------------------------|
| invert_channel Inverts | SIN and COS channel before the PGA for inverted output function (0 → SIN/COS, 1 → SINN/COSN) |
| cm_sin                 | Common mode voltage output enabled at SINN / CM pin (0 → differential, 1 → common)           |
| cm_cos                 | Common mode voltage output enabled at COSN / CM pin (0 → differential, 1 → common)           |
| gain                   | PGA gain setting (influences overall magnetic sensitivity), 2-bit                            |
| dc_offset              | Output DC bias offset (0 → Voffset1=1.5V, 1 → Voffset2=2.5V)                                 |
| Hall_b                 | Hall bias setting (influences overall magnetic sensitivity), 6-bit                           |

**Figure 16:**  
Sensitivity Gain Settings - Relative Sensitivity in %



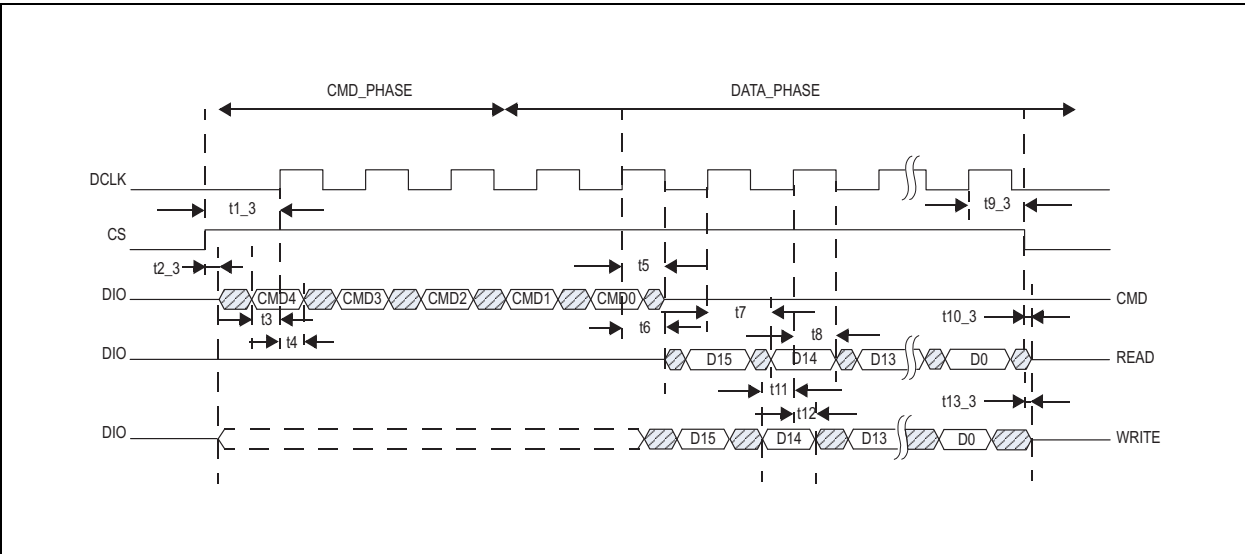
The amplitude of the output signal is programmable via sensitivity (6bit) and/or gain (2bit) settings (see [Figure 16](#)).

**Figure 17:**  
**Sensitivity Gain Settings - Sensitivity [mV/mT]**



**Waveform – Digital Interface at Normal Operation Mode**

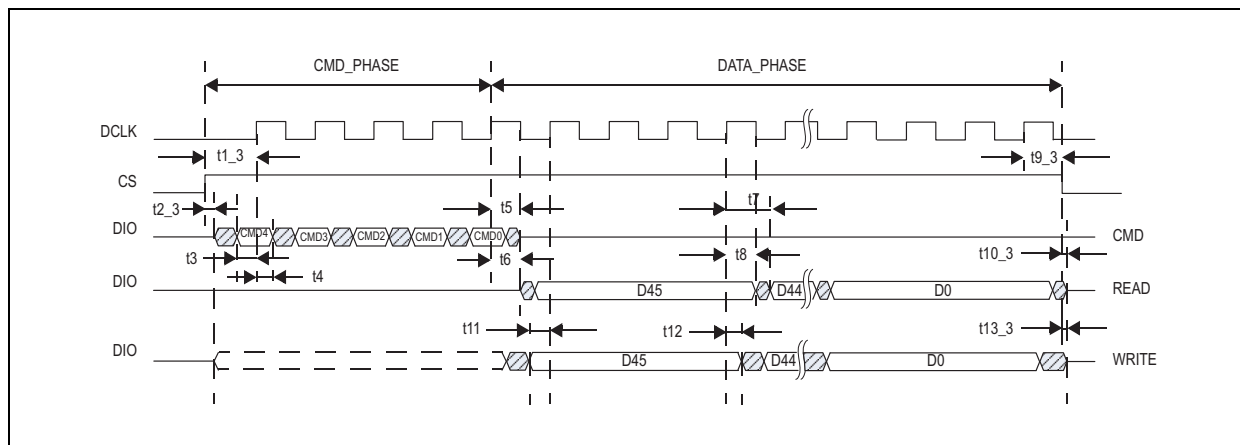
**Figure 18:**  
**Digital Interface at Normal Operation Mode**



## Waveform – Digital Interface at Extended Mode

In the extended mode, the digital interface needs four clocks for one data bit due to the internal structure. During this time, the device is able to handle internal signals for special access (e.g. the easy zap interface).

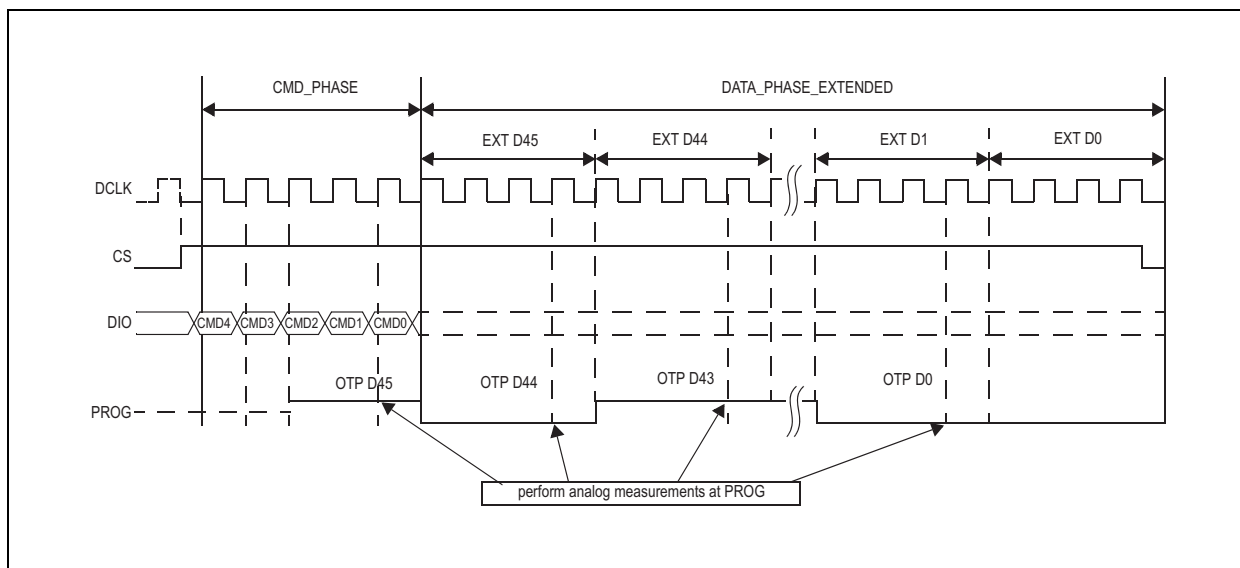
**Figure 19:**  
Digital Interface at Extended Mode



## Waveform – Digital Interface at Analog Readback of the Zener Diodes

To be sure that all Zener-Diodes are correctly burned, an analog readback mechanism is defined. Perform the 'READ OTP ANA' sequence according to the command table and measure the value of the diode at the end of each phase.

**Figure 20:**  
Digital Interface at Analog Readback of Zener Diodes



**Figure 21:**  
**Serial Bit Sequence (16-Bit Read/ Write)**

| Write Command |    |    |    |    | Read / Write Data |     |     |     |     |     |    |    |    |    |    |    |    |    |    |    |
|---------------|----|----|----|----|-------------------|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|
| C4            | C3 | C2 | C1 | C0 | D15               | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

### One Time Programming Content

The AS5115 die has an integrated 46-bit OTP ROM (Easyzap) for trimming and configuration purposes. The PROM can be programmed via the serial interface. For irreversible programming, an external programming voltage at PROG pin is needed. For security reasons, the factory trim bits can be locked by a lock bit.

As shown in the figure below, the OTP holds 46 bits. Bit number 44 and 45 are used for OTP testing purposes and ESD protection of the remaining cells.

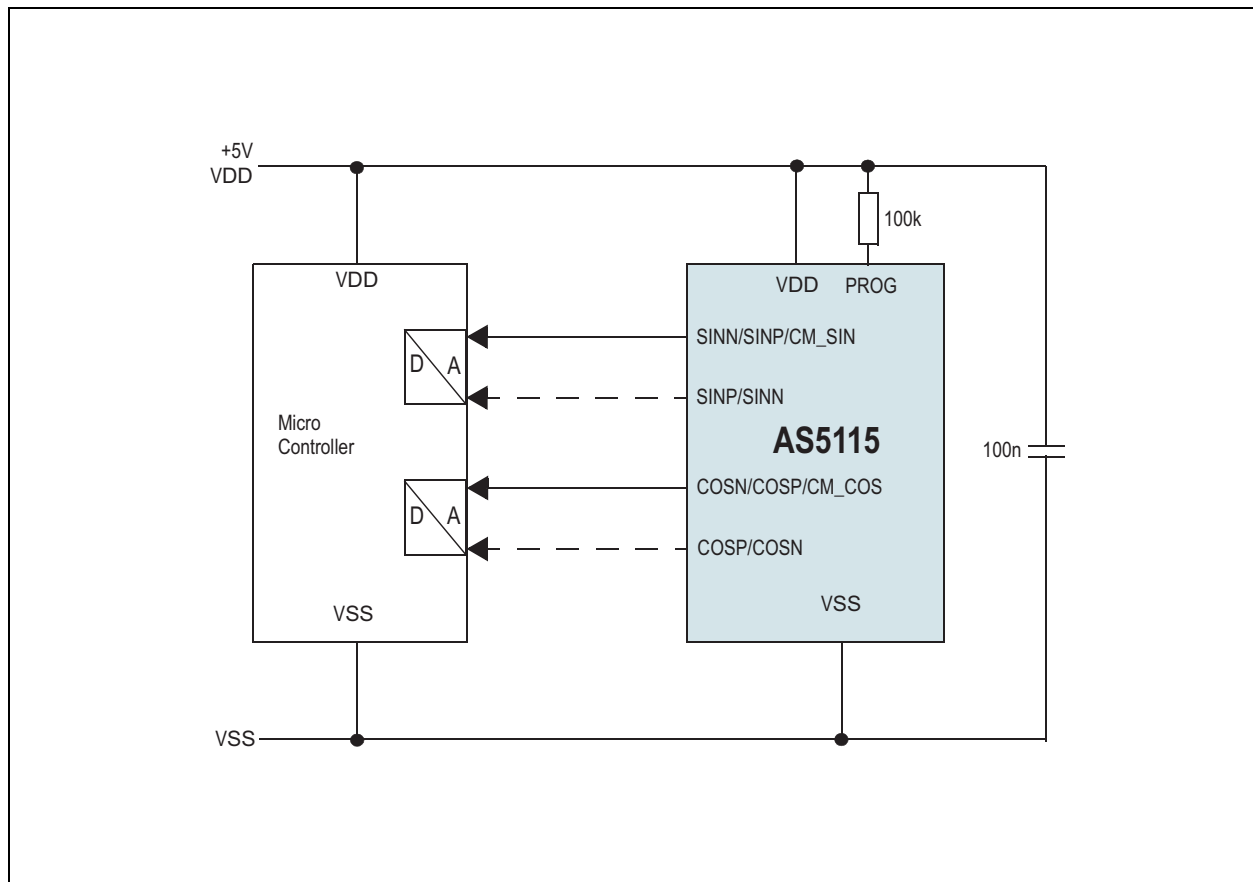
**Figure 22:**  
**OTP User Settings**

| Name           | Bit Count | OTP Start | OTP End | Access     | Comments                                                                |
|----------------|-----------|-----------|---------|------------|-------------------------------------------------------------------------|
| Hall_b         | 6         | 0         | 5       | User       | Sets overall sensitivity                                                |
| dc_offset      | 1         | 6         | 6       | User       | Output DC offset setting                                                |
| gain           | 2         | 7         | 8       | User       | Output Buffer Gain setting                                              |
| Lock           | 1         | 13        | 13      | <b>ams</b> | Set in production test                                                  |
| invert_channel | 1         | 11        | 11      | User       | Inverts SIN and COS channel before the PGA for inverted output function |
| cm_sin         | 1         | 10        | 10      | User       | Common mode voltage output enabled at SINN / CM pin                     |
| cm_cos         | 1         | 9         | 9       | User       | Common mode voltage output enabled at COSN / CM pin                     |

**Remark:** OTP assignment will be defined/updated.

## Analog Sin/Cos Outputs with External Interpolator

**Figure 23:**  
Sine and Cosine Outputs for External Angle Calculation



**Note(s):**

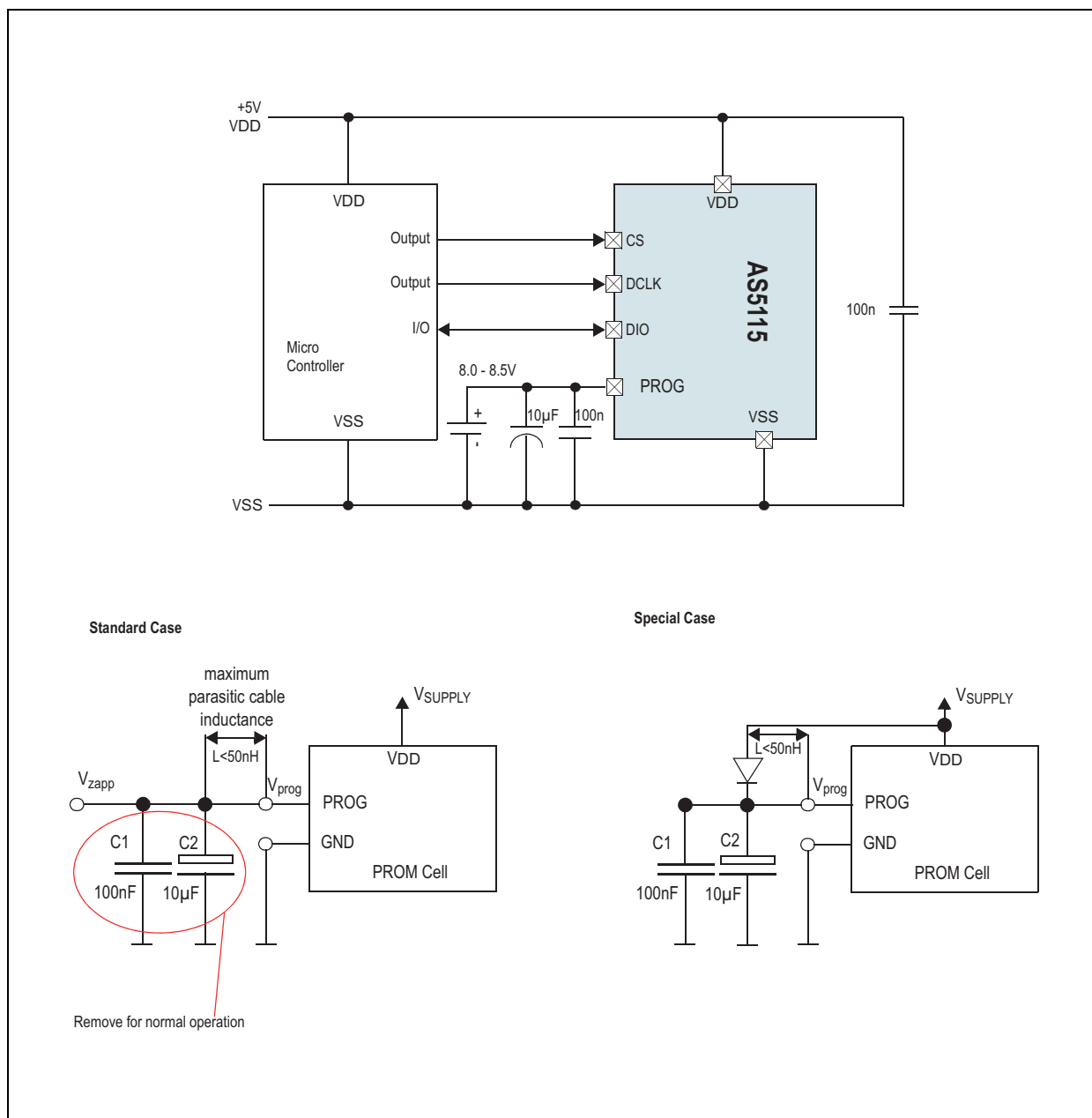
1. It is recommended to use a 100k pull-up resistance.
2. Default conditions for unused pins are: DCLK, CS, DIO, TC, A\_TST, TBO, TB1, TB2, TB3 connect to VSS.

The AS5115 provides analog sine and cosine outputs (SINP, COSP) of the Hall array front-end for test purposes. These outputs allow the user to perform the angle calculation by an external ADC +  $\mu$ C, e.g. to compute the angle with a high resolution. The signal lines must be kept as short as possible. In the case of longer lines, they must be shielded in order to achieve best noise performance.

Through the programming of one bit, you have the possibility to choose between the analog sine and cosine outputs (SINP, COSP) and their inverted signals (SINN, COSN). Furthermore, by programming the bits <9:10> you can enable the common mode output signals of SIN and COS.

## OTP Programming and Verification

**Figure 24:**  
OTP Programming Connection



**Note(s):**

1. The maximum capacitive load at PROG in normal operation should be less than 20pF. However, during programming the capacitors C1+C2 are needed to buffer the programming voltage during current spikes, but they must be removed for normal operation. To overcome this contradiction, the recommendation is to add a diode (4148 or similar) between PROG and VDD as shown in Figure 24 (special case setup), if the capacitors can not be removed at final assembly. Due to D1, the capacitors C1+C2 are loaded with  $V_{DD} - 0.7\text{V}$  at startup, hence not influencing the readout of the internal OTP registers. During programming the OTP, the diode ensures that no current is flowing from PROG (8V - 8.5V) to VDD (5V). In the standard case (see Figure 24), the verification of a correct OTP readout can be done by analog readback of the OTP register. As long as the PROG pin is accessible it is recommended to use standard setup. In case the PROG pin is not accessible at final assembly, the special setup is recommended.

For programming of the OTP, an additional voltage has to be applied to the pin PROG. It has to be buffered by a fast 100nF capacitor (ceramic) and a 10μF capacitor. The information to be programmed is set by command 25. The OTP bits 16 until 45 are used for **ams** factory trimming and cannot be overwritten.

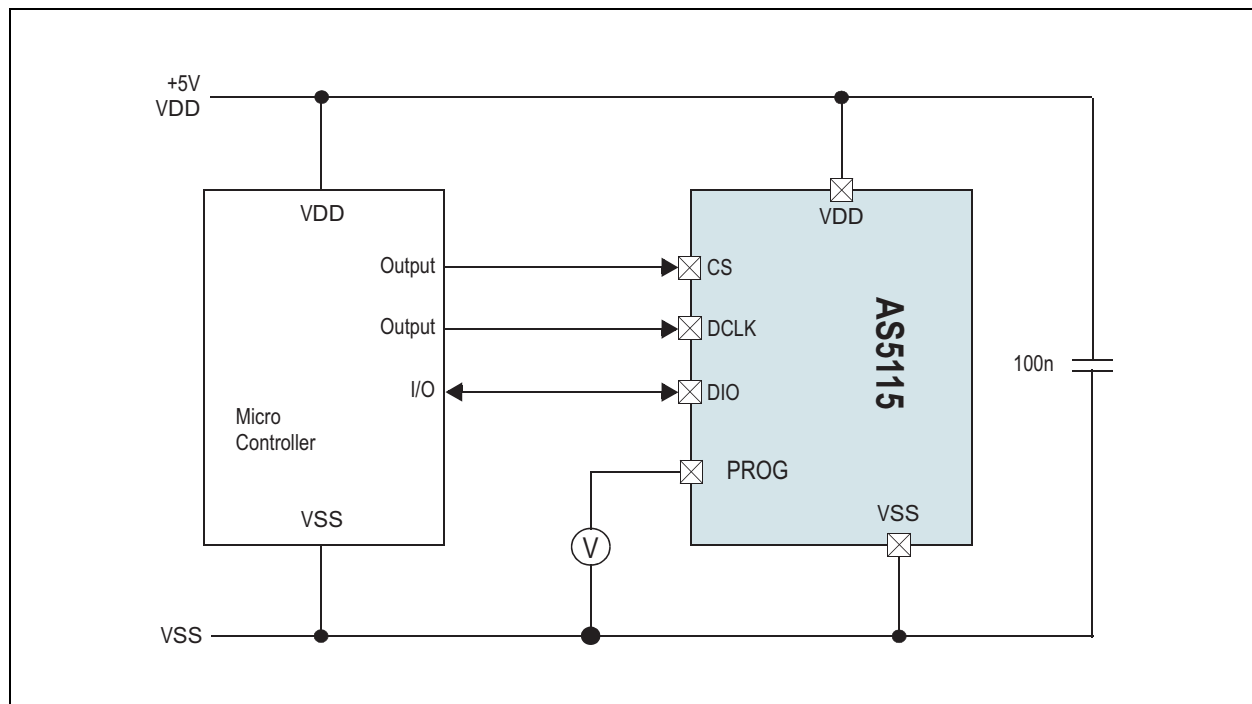
**Figure 25:**  
**OTP Programming Parameters**

| Symbol            | Parameter           | Min | Max | Unit | Note        |
|-------------------|---------------------|-----|-----|------|-------------|
| V <sub>DD</sub>   | Supply Voltage      | 5   | 5.5 | V    |             |
| GND               | Ground Level        | 0   | 0   | V    |             |
| V <sub>zapp</sub> | Programming Voltage | 8   | 8.5 | V    | At pin PROG |
| T <sub>zapp</sub> | Temperature         | 0   | 85  | °C   |             |
| f <sub>clk</sub>  | CLK Frequency       |     | 100 | kHz  | At pin DCLK |

After programming, the programmed OTP bits have to be verified by Analog Verification:

By switching into Extended Mode and sending an ANALOG OTP READ command (#9), pin PROG becomes an output, sending an analog voltage with each clock representing a sequence of the bits in the OTP register (starting with D45). A voltage of <500mV indicates a correctly programmed bit ("1") while a voltage level between 2V and 3.5V indicates a correctly unprogrammed bit ("0"). Any voltage level in between indicates incorrect programming.

**Figure 26:**  
**Analog OTP Verification**



### Pre-Programmed Version

**Figure 27:**  
**Pre-Programmed Version**

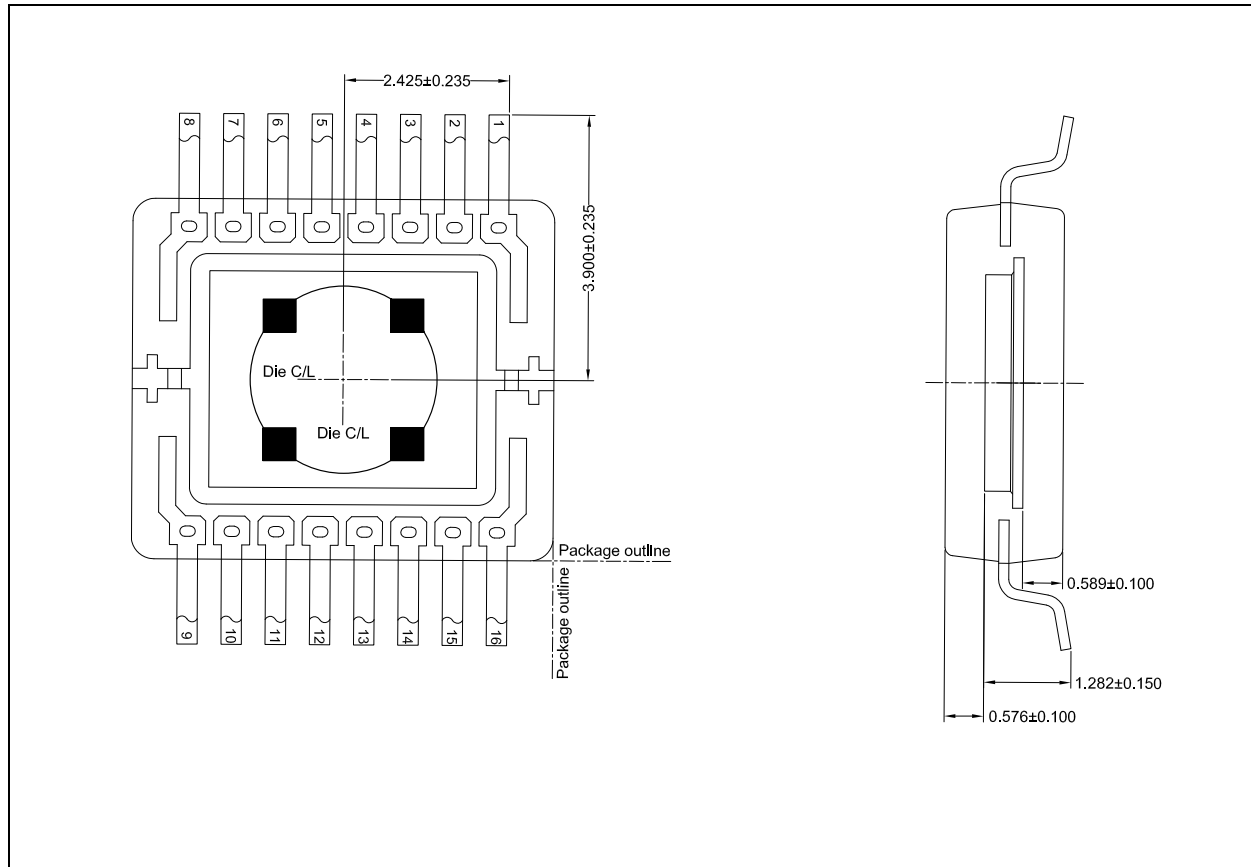
| Version | Sensitivity    | Output | Output DC Offset | PGA Gain Setting | Hall Bias Current                 |
|---------|----------------|--------|------------------|------------------|-----------------------------------|
| AS5115  | Not programmed | 1.5V   | 0                | Not programmed   | Untrimmed                         |
| AS5115A | 28 mV/mT       | 2.5V   | 1                | 00               | 14μA                              |
| AS5115F | 24 mV/mT       | 1.5V   | 0                | 11               | 8.42μA<br>(trim code 10hex fixed) |

## Application Information

### Mechanical Data

The internal Hall elements are placed in the center of the package on a circle with a radius of 1 mm.

**Figure 28:**  
**Hall Element Position**



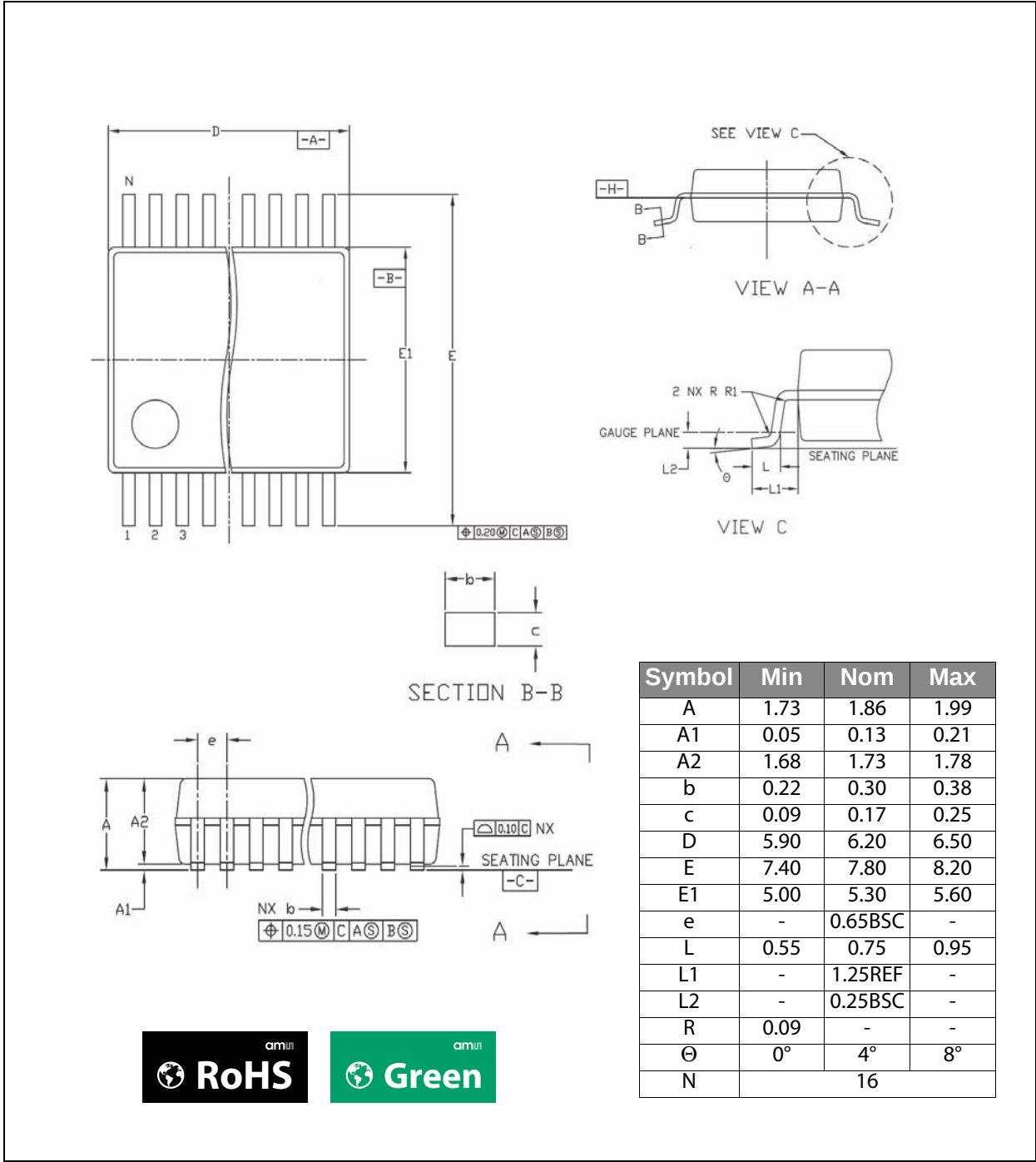
**Note(s):**

1. All dimensions in mm.
2. Die thickness  $381\mu\text{m}$ .
3. Adhesive thickness  $30 \pm 15\mu\text{m}$ .
4. Leadframe downset  $200 \pm 38\mu\text{m}$ .
5. Leadframe thickness  $152 \pm 8\mu\text{m}$ .

Package Drawings & Markings

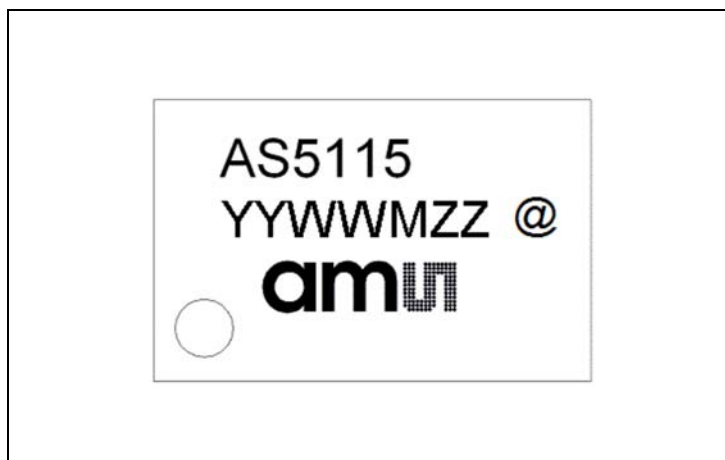
The devices are available in a 16-lead shrink small outline package.

Figure 29:  
Package Drawings and Dimensions

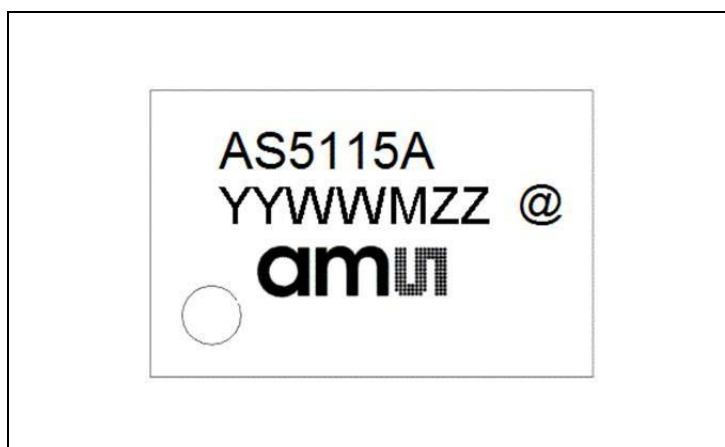


- Note(s):**
1. Dimensions and tolerancing conform to ASME Y14.5M-1994.
  2. All dimensions are in millimeters. Angles are in degrees.

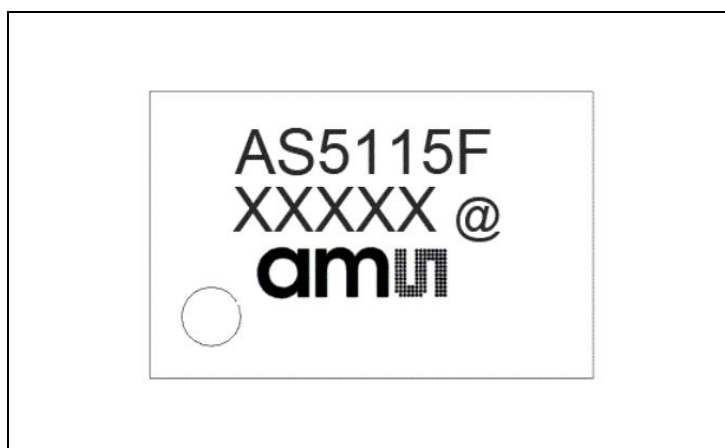
**Figure 30:**  
AS5115 Marking



**Figure 31:**  
AS5115A Marking



**Figure 32:**  
AS5115F Marking



**Figure 33:**  
**AS5115/AS5115A Package Code**

| YY                                        | WW                 | M                | ZZ                         | @                 |
|-------------------------------------------|--------------------|------------------|----------------------------|-------------------|
| Last two digits of the manufacturing year | Manufacturing week | Plant identifier | Assembly traceability code | Sublot identifier |

**Figure 34:**  
**AS5115F Package Code**

| XXXXX     |
|-----------|
| Tracecode |

## Ordering & Contact Information

The devices are available as the standard products shown in Figure 35.

**Figure 35:**  
**Ordering Information**

| Ordering Code | Package | Marking | Delivery Form               | Delivery Quantity |
|---------------|---------|---------|-----------------------------|-------------------|
| AS5115-HSST   | SSOP-16 | AS5115  | 13" Tape & Reel in dry pack | 2000 pcs/reel     |
| AS5115-HSSM   | SSOP-16 | AS5115  | 7" Tape & Reel in dry pack  | 500 pcs/reel      |
| AS5115A-HSSP  | SSOP-16 | AS5115A | 13" Tape & Reel in dry pack | 2000 pcs/reel     |
| AS5115A-HSSM  | SSOP-16 | AS5115A | 7" Tape & Reel in dry pack  | 500 pcs/reel      |
| AS5115F-HSSP  | SSOP-16 | AS5115F | 13" Tape & Reel in dry pack | 2000 pcs/reel     |

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| Document Status          | Product Status  | Definition                                                                                                                                                                                                                                                         |
|--------------------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Preview          | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice                                                                    |
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## Revision Information

| Changes from 1-15 (2016-Feb-02) to current revision 1-16 (2016-Nov-17) | Page |
|------------------------------------------------------------------------|------|
| Updated Figure 5                                                       | 5    |
| Updated text under Figure 25                                           | 20   |
| Updated Figure 27                                                      | 21   |

### Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

## Content Guide

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